A Semblance of Manual Regulation

Turning this Circuit OFF

When capacitor, C8, is precharged with 10V and the resistor labeled “choke” is reduced to one-tenth of a solder joint or less (≤10μΩ), then this circuit behaves in a conventional manner. The waveform of the current source (representing a ferromagnetizable armature in which is embedded a self-looped copper wire of 0000 AWG) becomes manifest and the total power of generation is nearly equal to zero watts if the total power of the entire circuit’s dissipation and storage of power is subtracted from the total power of the circuit’s generation.

All of this tells me that, in order to regulate the “overunity” condition of this circuit by precluding it from occurring, one way of doing this is to reduce the resistance of the “choke” to one-tenth of the resistance of a solder joint in order to turn OFF overunity to facilitate the drainage of any accumulation of power located anywhere within this circuit.

The “choke” is located at the top, and in the center, of the following schematic...

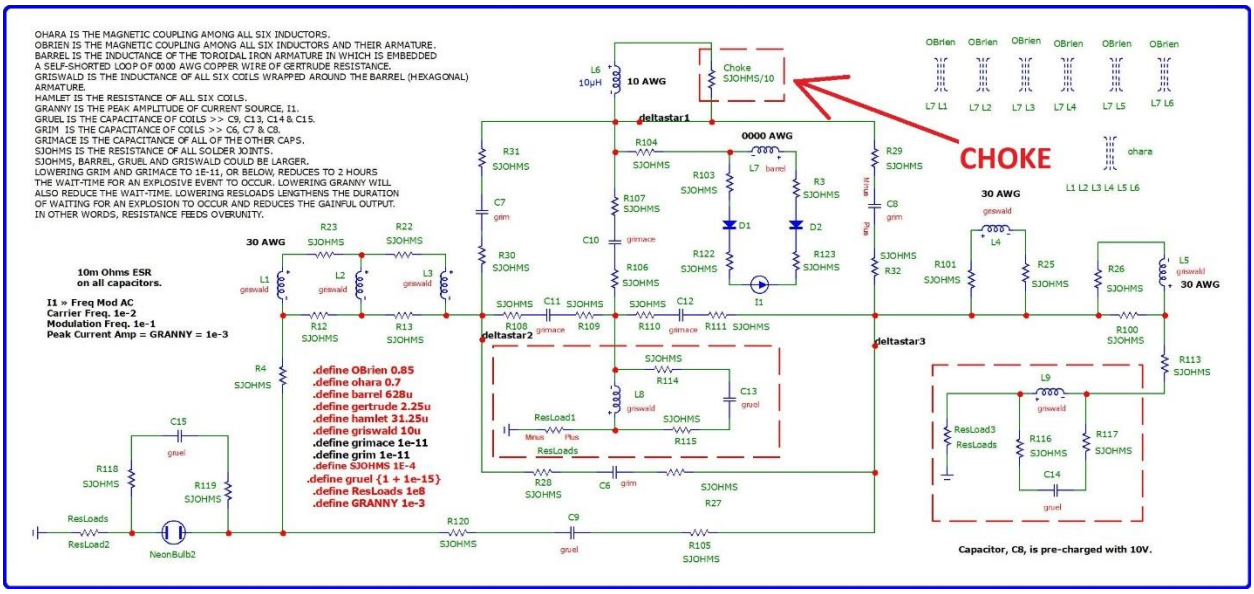

Figure 1 - Schematic with the regulatory “choke”.

The output of this circuit, under this condition, illustrates conventional behavior which is expected to comply with entropy while nonlinear influences are not in evidence.

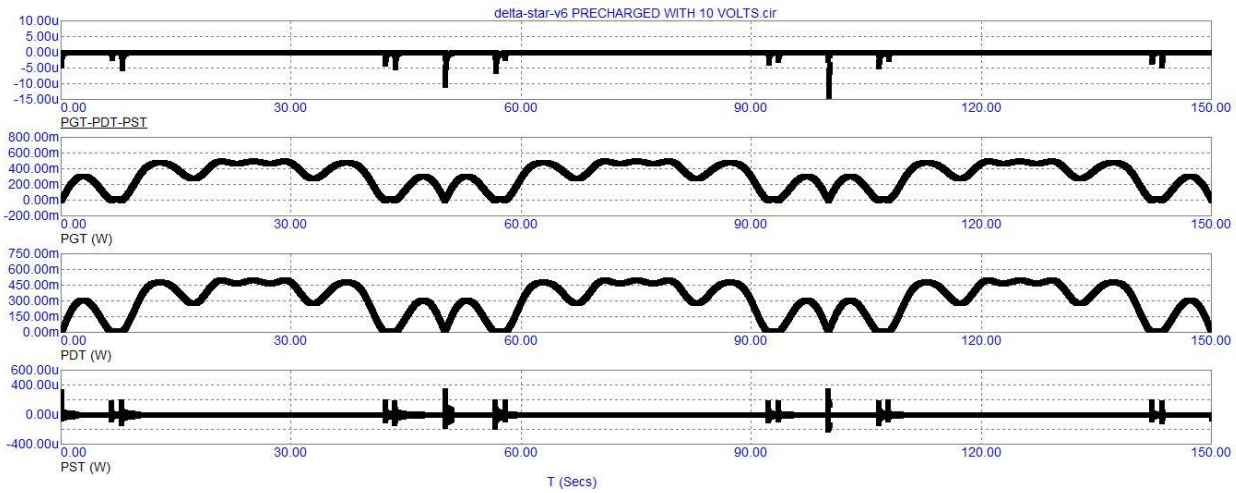

Figure 2 - Conventional output with some spikes in the first graph indicating the generation of residual power remaining after we've subtracted the dissipation and the storage of power.

In other words, if we subtract the total dissipation of power and the total storage of power from the total generation of power in the first graph at the top of the virtual oscilloscope tracings in the screenshot up-above, then we get a value which approaches zero as time passes except for a transient surge of power generation which supersedes the dissipation and the storage of power at the onset of the simulator's runtime (indicated by a spike of power proceeding downwards in the negative direction approaching a peak of negative one and one-half microwatts in graph #1).

You'll notice that the second and third graphs exhibit the characteristic waveform pattern of the frequency modulated A/C output of the current source (which this simulation is using to represent the armature), in combination with a self-shorted copper loop described up-above.

Here are some more renditions of this circuit's output...

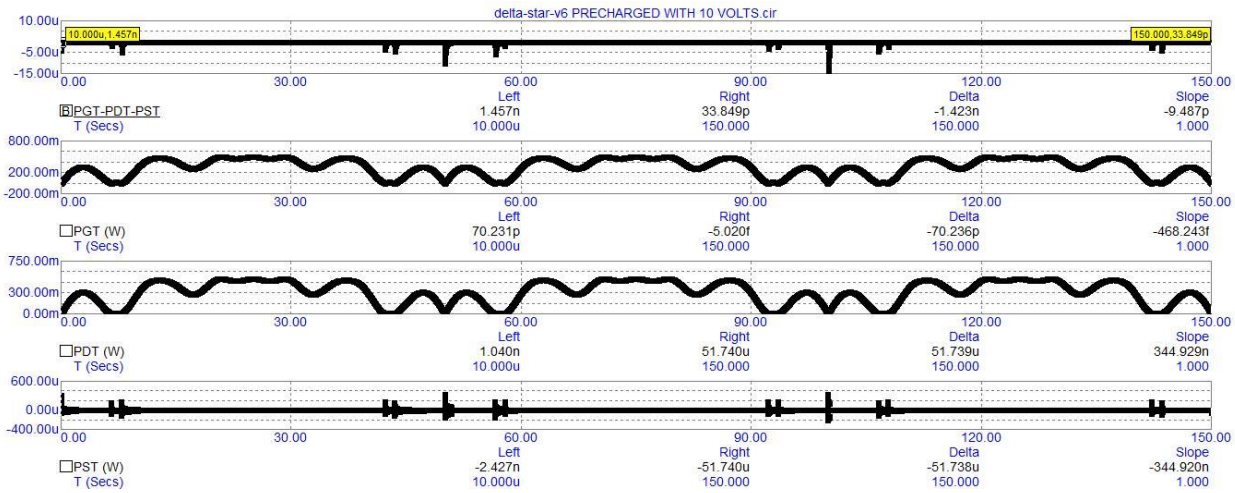

Figure 3 - Conventional output with numeric data.

Upon this armature is wound the six coils which are electrically connected, each in parallel, with the three capacitors, C6 & C7 & C8, which are arranged in a delta (triangular) formation.

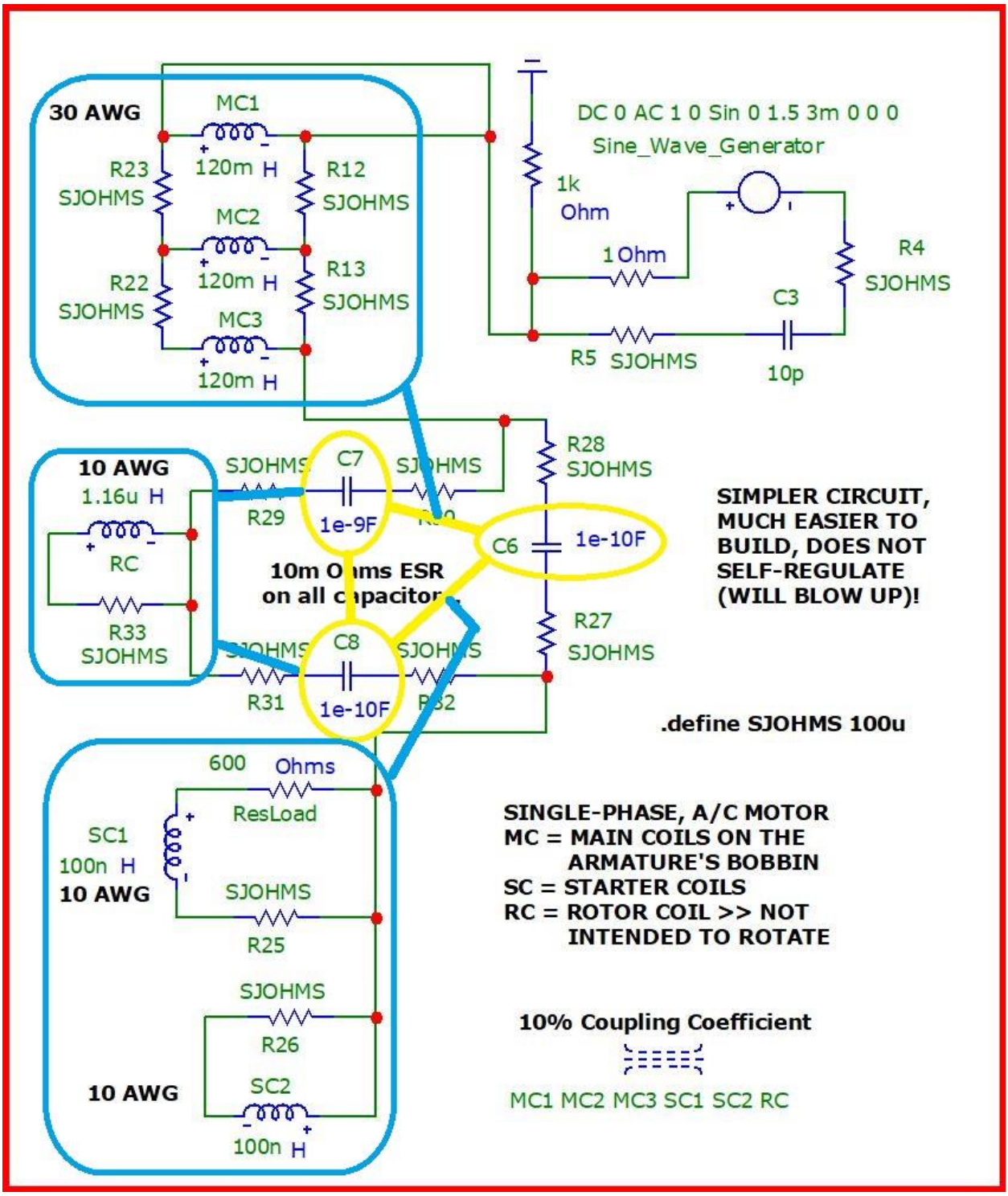

Figure 4 - A delta formation of an earlier rendition of a triangular (delta) Bewley Archetype (in yellow) with parallel inductances (in blue).

And within this triangular ring of capacitors is connected a star (wye) formation of three additional capacitors.

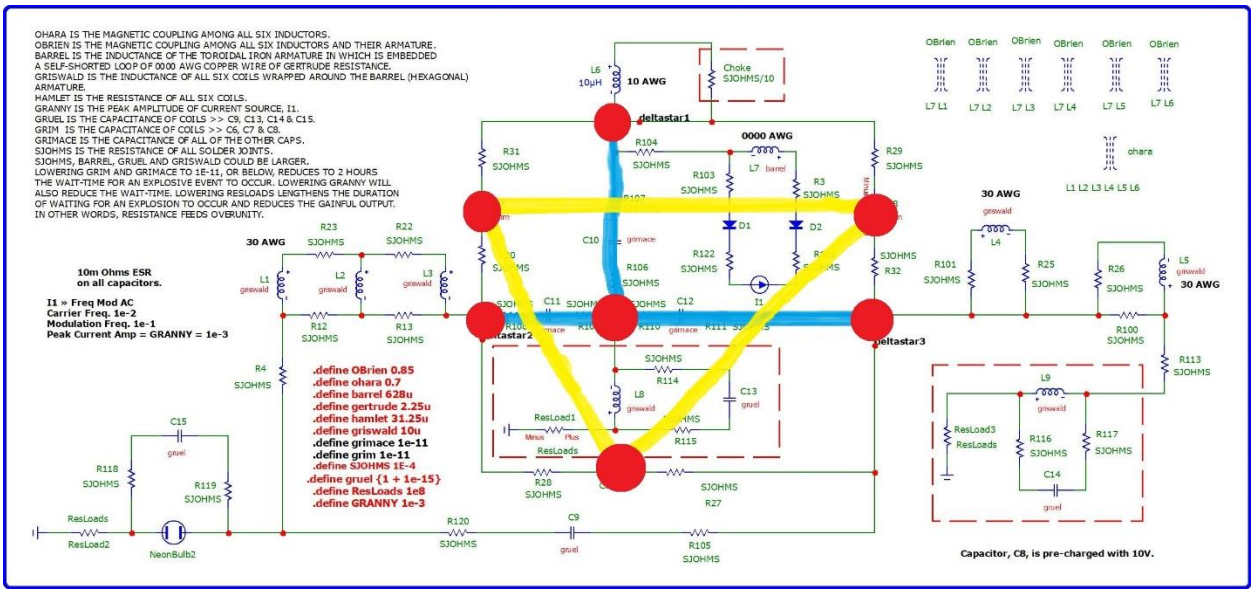

Figure 5 - A hexagonal highlight of the delta-star version of a Bewley Archetype.

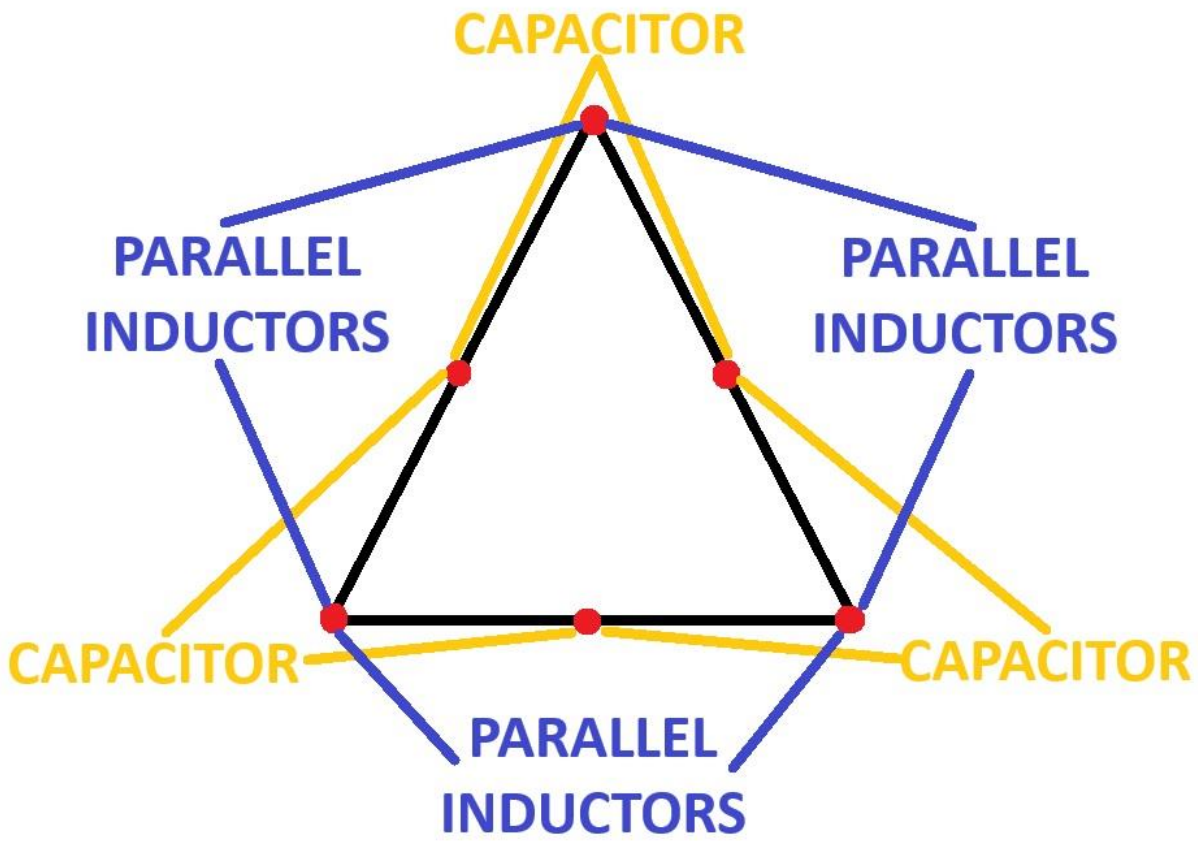

Figure 6 - A symbolic representation of a delta-star formation of a Bewley Archetype.

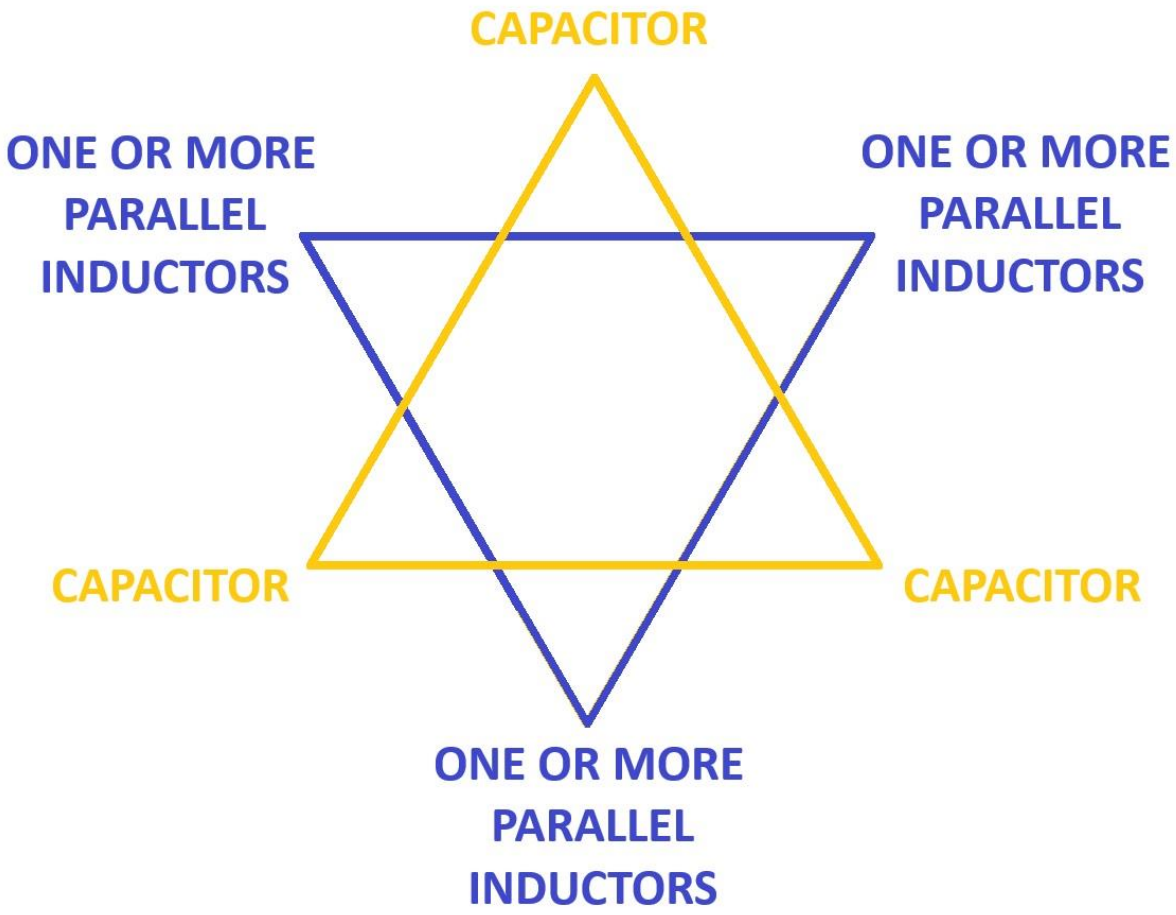

Figure 7 - Same as figure #6, but this is tidied up a bit.

The archetypal formation of a Bewley Archetype, up-above, is hexagonal. Yet, my earlier rendition of this archetype was rectangular. Here is its proto-formation...

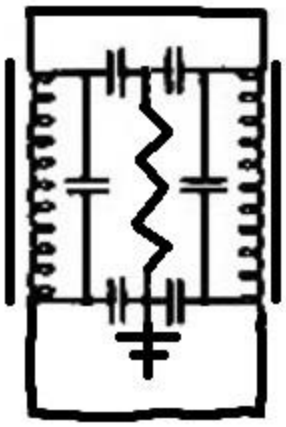

Figure 8 - A proto-formation of a rectangular archetype of a Bewley transmission network, ala Eric Dollard's analog computer in LMD mode.

And its subsequent simplification…

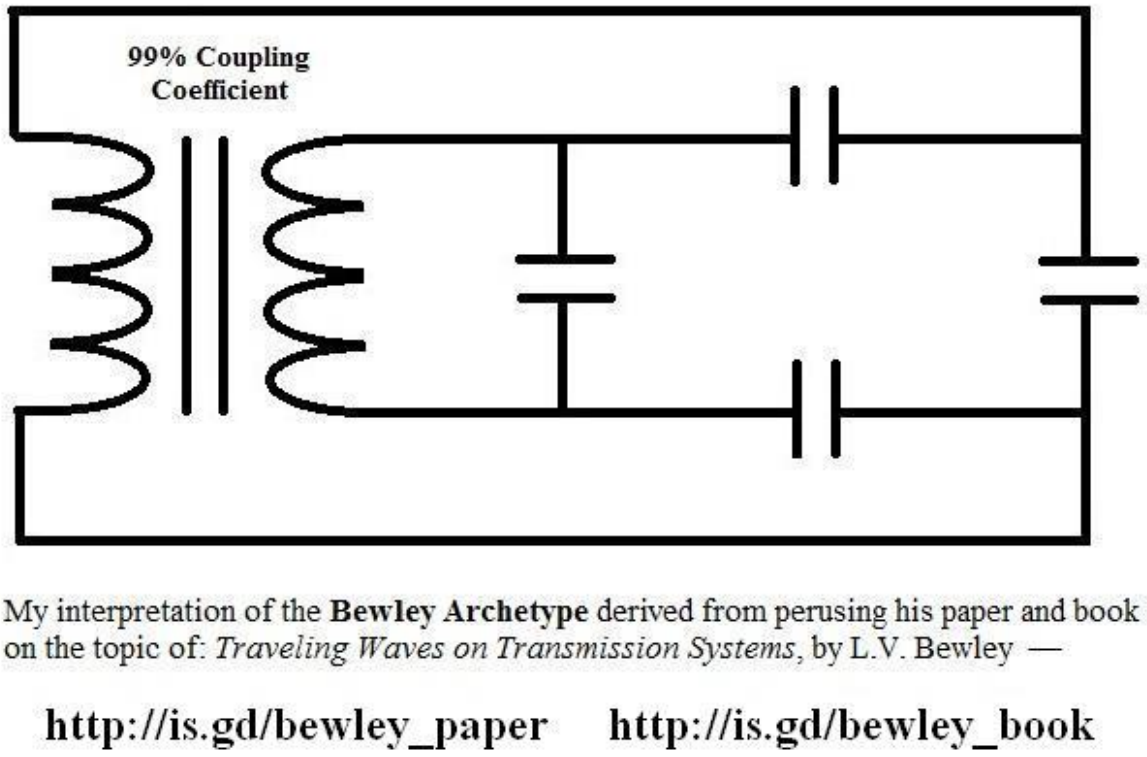

Figure 9 - An archetypal simplification of my proto-derivation of a Bewley Archetype.

These six capacitors are my most recent rendition of a “Bewley Archetype” exhibiting the characteristics of emphasizing capacitance in series and inductance in parallel within a

synthetic (analogous) transmission network (worthy of bench-testing) inspired by Eric P. Dollard's analog computer of a transmission network in longitudinal magneto-dielectric mode (LMD).

This is in contrast to a conventional transmission network in which inductance is in series and capacitance is in parallel within a pair of transmission lines stretching down the length of the numerous segments of their network (as exhibited in the following diagram) ...

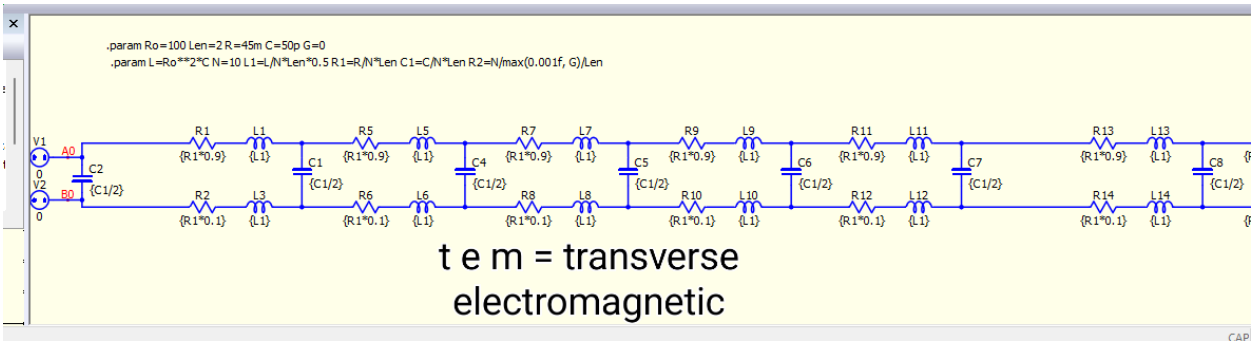

Figure 10 - Someone else's rendition of a TEM (transverse electromagnetic) network of Eric Dollard's analog computer in TEM mode.

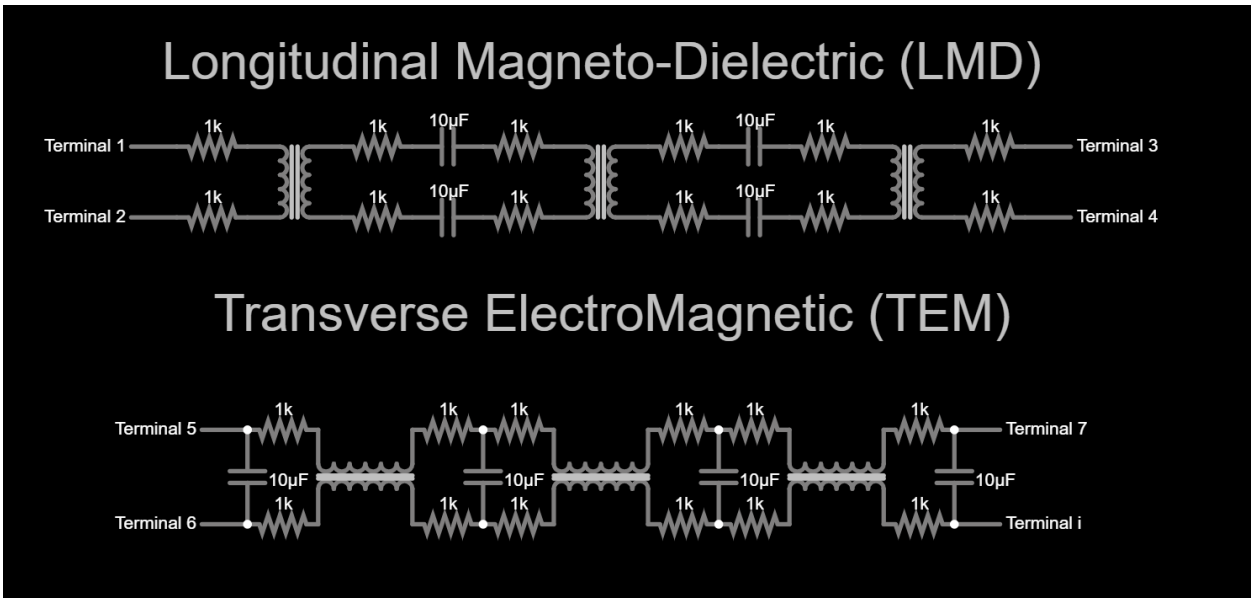

Figure 11 - https://tinyurl.com/temvslmd

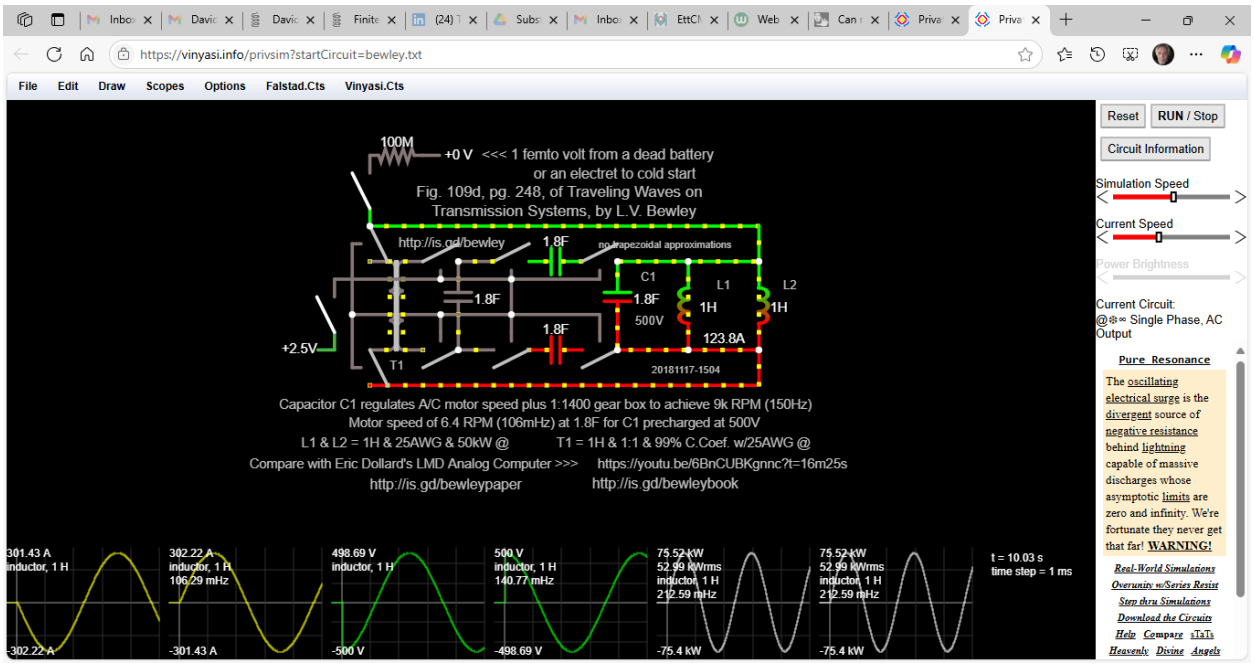

Figure 12 - https://vinyasi.info/privsim?startCircuit=bewley.txt

Here are some more screenshots of the nodal voltages of figures #1 and #5...

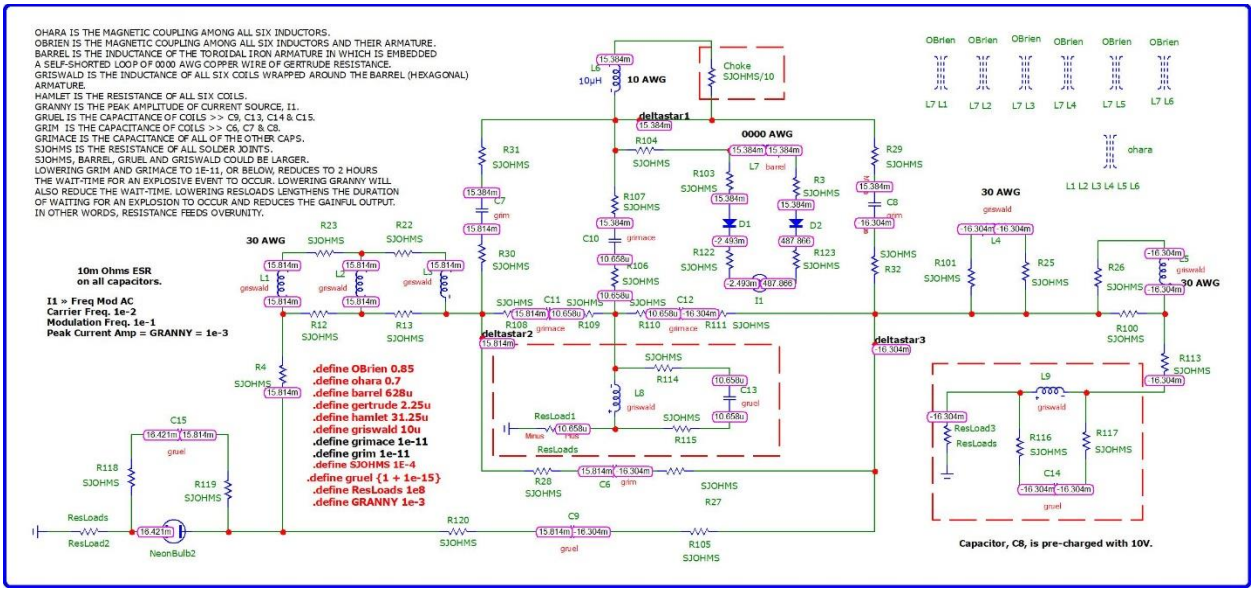

Figure 13 - Nodal voltages.

And its currents...

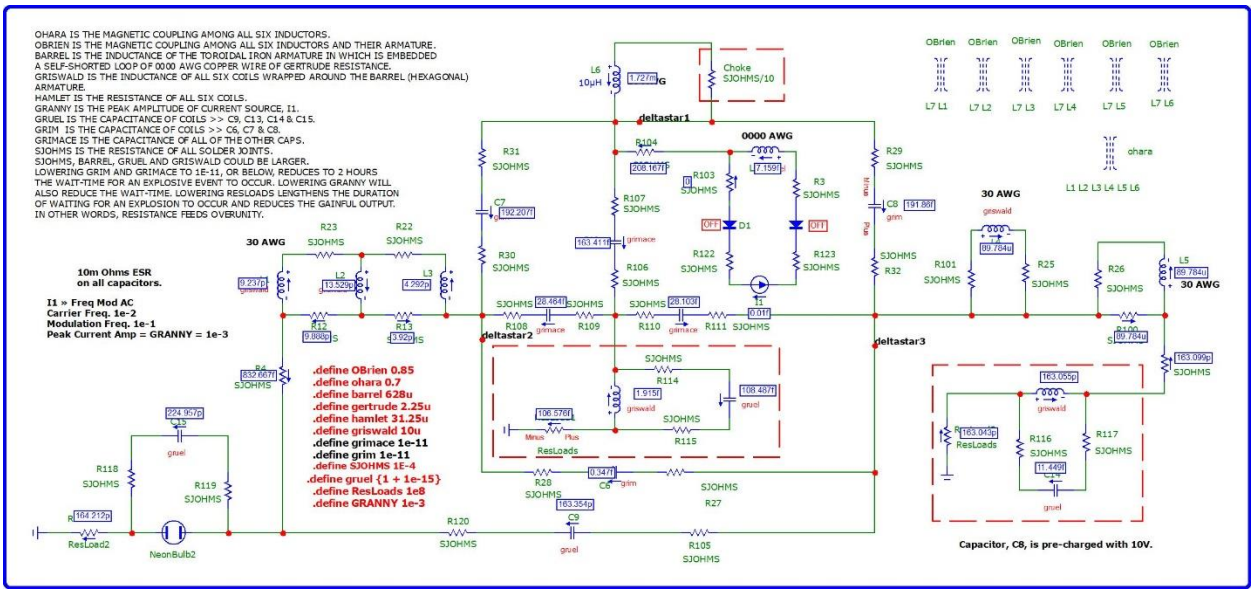

Figure 14 - Currents and the condition of the diodes (they are OFF).

Oddly enough, I had to get through the harder method to discover an easier way...!...is to add a ground through a resistive valve of 1kΩ so as to neutralize the impact which the choke resistor of 1e10Ω would otherwise have if this extra grounded pathway had not been included.

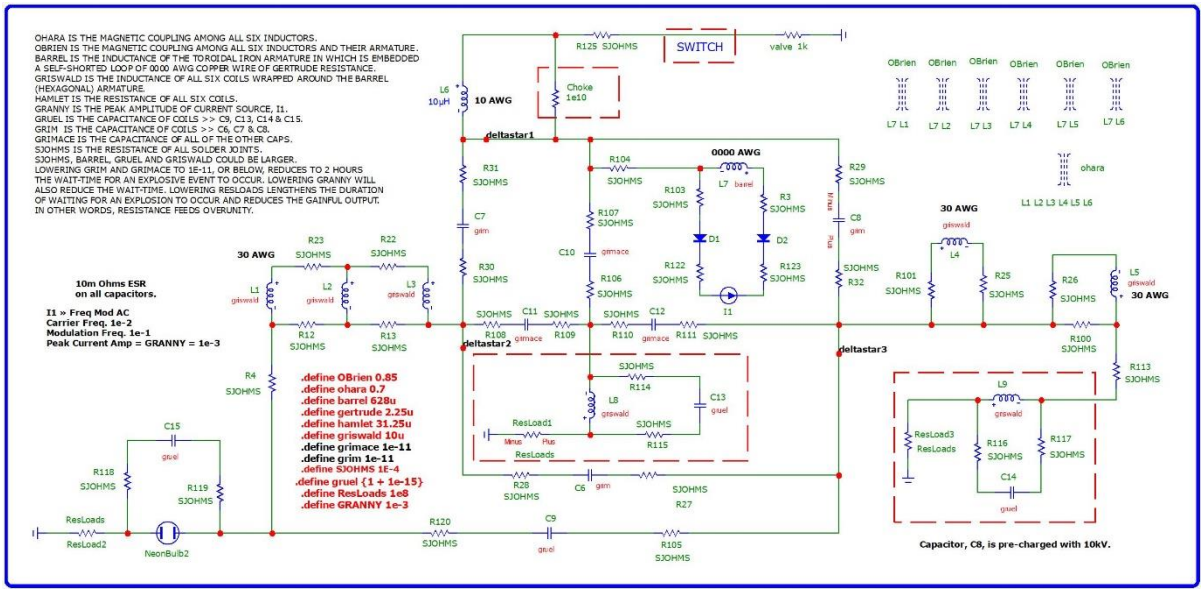

Figure 15 - Choke is grounded so as to neutralize its influence.

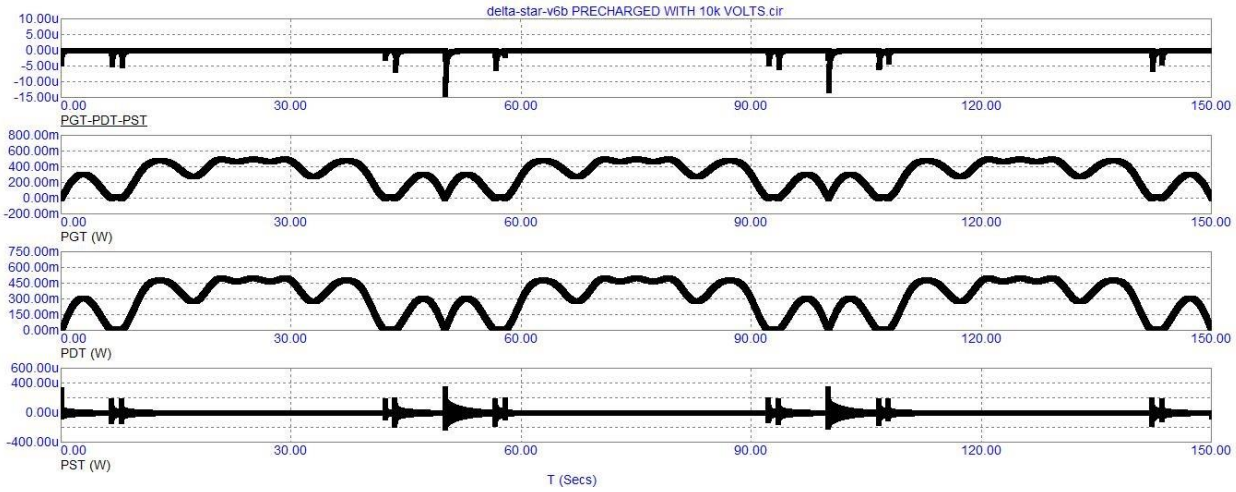

Figure 16 - Output with a grounded choke is able to withstand a precharged condition of 10kV.

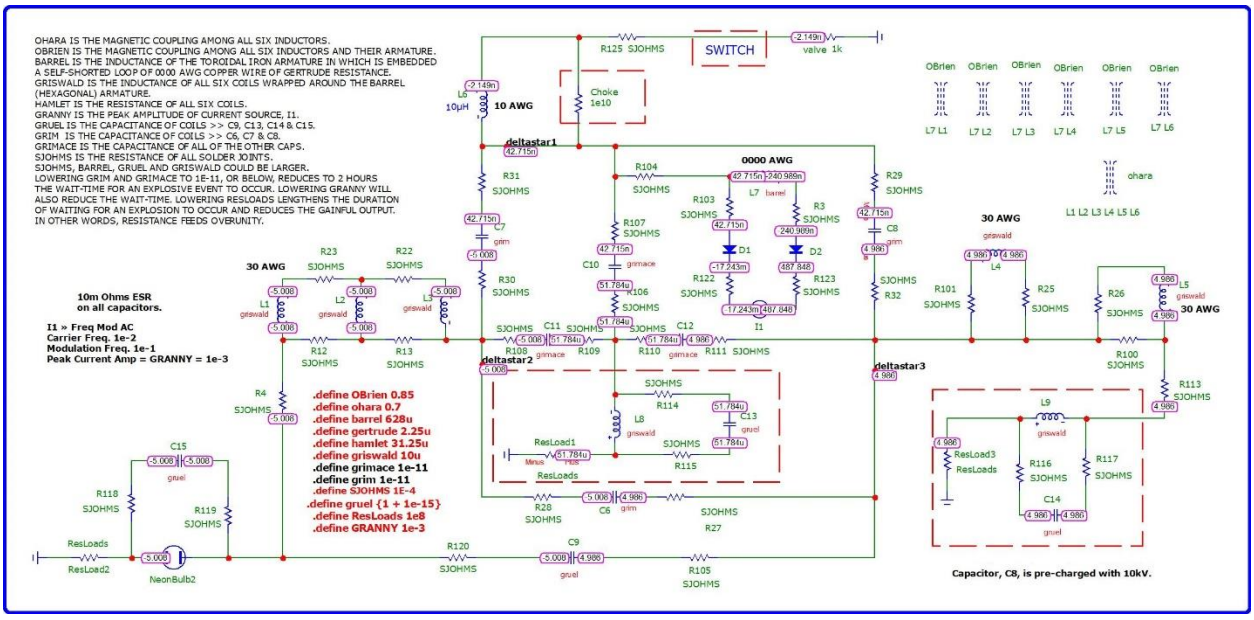

Figure 17 - Nodal voltages.

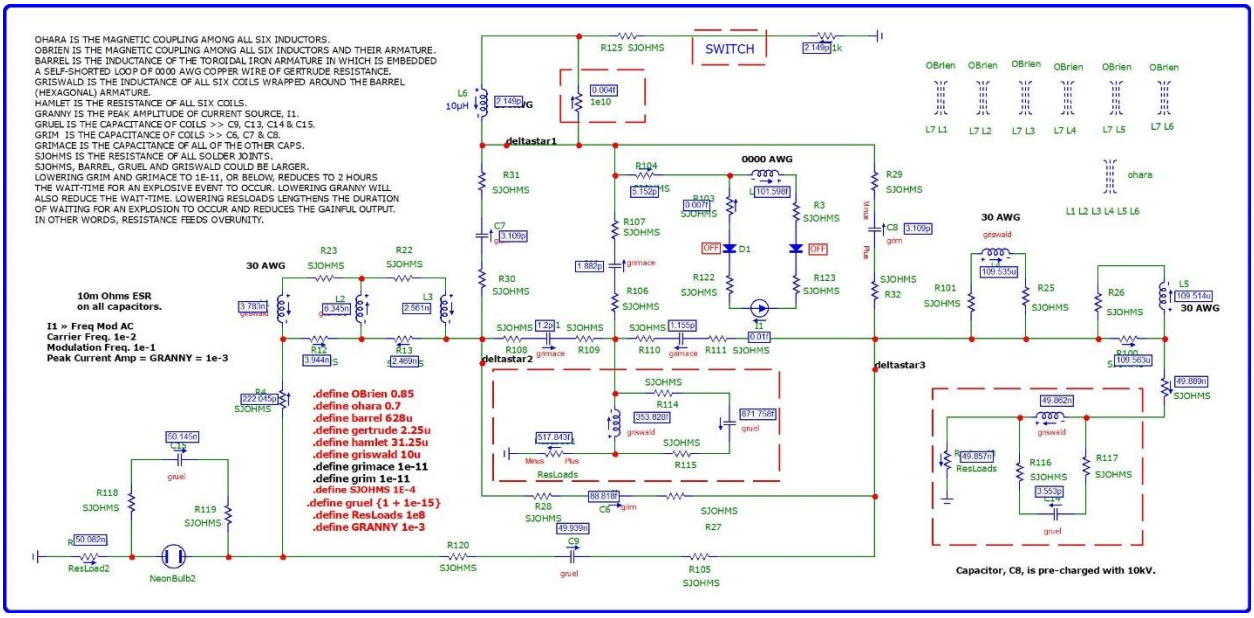

Figure 18 - Currents and the condition of the diodes (they are OFF).