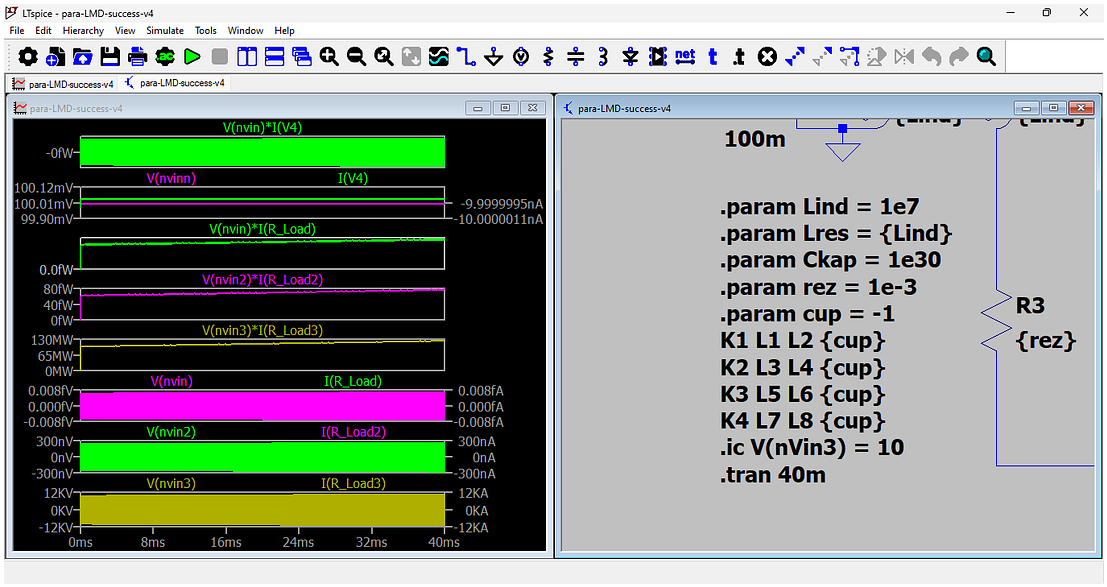
Parametric LMD, success, v4!

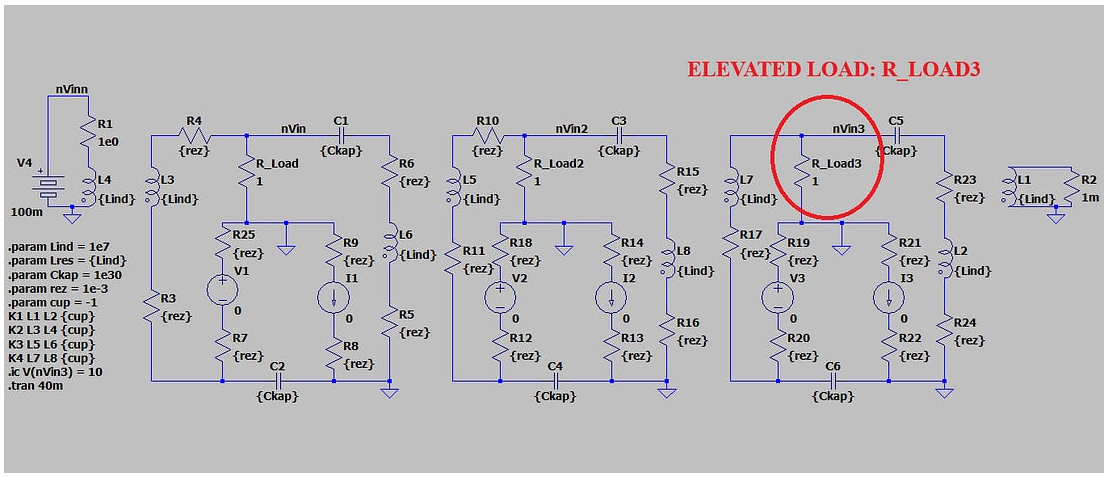
EUREKA

VINYASI

APR 29, 2026



You'll notice, in the screenshot above, that the input wattage in the topmost graph is so low that LTSpice fails to measure it in any units that the simulator is aware of. Meanwhile, the bottom-most graph, of R_Load3, is considerably elevated by comparison to all the others which is no surprise since that's where the 10 volt precharged capacitor is located adjacent to node 'nVin3'.



If the precharged node/capacitor is moved over to ‘nVin2’, a much larger explosion of power occurs. But the simulation is halted with an error message:

> Warning: Simulation tolerance relaxed to achieve convergence from 3.2053254174741815e-07 to 3.2053254174741815e-07 seconds.

… suggesting that this is not the right place to put the precharged node. Any other location may also give errors but does not encourage a healthy response of elevated power (at all), anywhere, throughout the circuit.

And if the battery, V4 on the far left, is reduced to zero volts of input, then errors also occur suggesting that its presence helps to stabilize the operation of the simulator’s calculating engine — which I take to be suggestive of reducing the stress of any circuit in the real world as well as the virtual world of the simulator.

I think this version qualifies as a successful demonstration that Eric Dollard’s LMD modality of a transmission line favors longitudinal waves over transverse.

What else could it be that is germane to my intention of demonstrating filtration (blockage) of TEM? Practicality or common sense are not my objectives. So, I let loose with my parameters knowing it doesn't matter if it appears to become non-buildable by current standards.

I added solder joints which is what spurred me onward to tweak the other parameters "any which way I could" to get satisfactory results.

Here's the Netlist > > >

* C:\Users\vinya\Documents\Sims\LTSpice\2026\04 - Apr\28\para-LMD-success-v4.asc

* Generated by LTspice 24.1.9 for Windows.

R_Load nVin 0 1

L1 N007 0 {Lind} Rser={Lres}

L2 N012 N022 {Lind} Rser={Lres}

C1 N002 nVin {Ckap}

C2 0 N029 {Ckap}

L3 N001 N019 {Lind} Rser={Lres}

L4 N006 0 {Lind} Rser={Lres}

R2 N007 0 1m

I1 N014 N028 0

V1 N013 N023 0

R_Load2 nVin2 0 1

L5 N003 N010 {Lind} Rser={Lres}

C3 N004 nVin2 {Ckap}

C4 0 N030 {Ckap}

L6 N008 N020 {Lind} Rser={Lres}

I2 N016 N025 0

V2 N015 N024 0

R_Load3 nVin3 0 1

C5 N005 nVin3 {Ckap}

C6 0 N031 {Ckap}

L7 nVin3 N009 {Lind} Rser={Lres}

I3 N018 N027 0

V3 N017 N026 0

L8 N011 N021 {Lind} Rser={Lres}

V4 nVinn 0 100m

R1 nVinn N006 1e0

R3 N019 N029 {rez}

R4 nVin N001 {rez}

R5 N020 0 {rez}

R6 N002 N008 {rez}

R7 N023 N029 {rez}

R8 N028 0 {rez}

R9 0 N014 {rez}

R10 nVin2 N003 {rez}

R11 N010 N030 {rez}

R12 N024 N030 {rez}

R13 N025 0 {rez}

R14 0 N016 {rez}

R15 N004 N011 {rez}

R16 N021 0 {rez}

R17 N009 N031 {rez}

R18 0 N015 {rez}

R19 0 N017 {rez}

R20 N026 N031 {rez}

R21 0 N018 {rez}

R22 N027 0 {rez}

R23 N005 N012 {rez}

R24 N022 0 {rez}

R25 0 N013 {rez}

.param Lind = 1e7

.param Lres = {Lind}

.param Ckap = 1e30

.param rez = 1e-3

.param cup = -1

K1 L1 L2 {cup}

K2 L3 L4 {cup}

K3 L5 L6 {cup}

K4 L7 L8 {cup}

.ic V(nVin3) = 10

.tran 40m

.backanno

.end

Here’s the log file > > >

LTspice 24.1.9 for Windows

Circuit: C:\Users\vinya\Documents\Sims\LTSpice\2026\04 - Apr\28\para-LMD-success-v4.net

Start Time: Tue Apr 28 18:41:36 2026

solver = Normal

Maximum thread count: 4

tnom = 27

temp = 27

method = trap

Direct Newton iteration for .op point succeeded.

Total elapsed time: 0.279 seconds.

Files loaded:

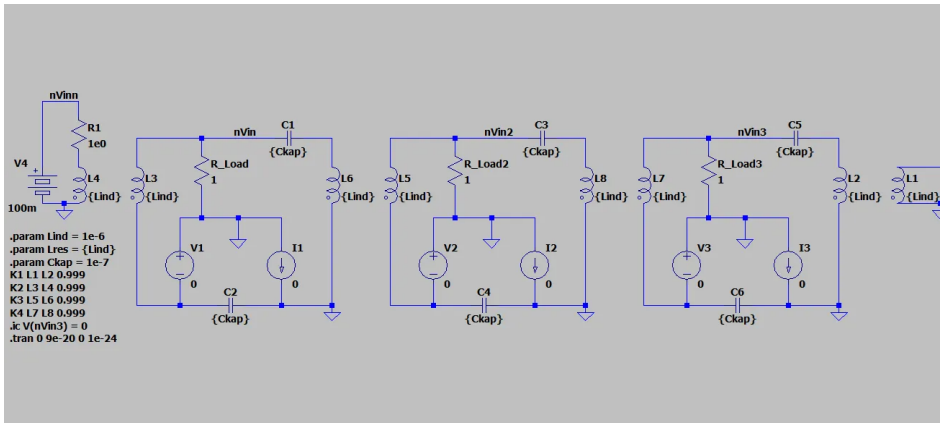
C:\Users\vinya\Documents\Sims\LTSpice\2026\04 - Apr\28\para-LMD-success-v4.net

Here's the download link.

Here's the prior post:

Parametric LMD, success, v3?

VINYASI · APR 28



Schematic:

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