Don Smith Without the Charged Barrier of William Jay Fogal! No Central Transistor.

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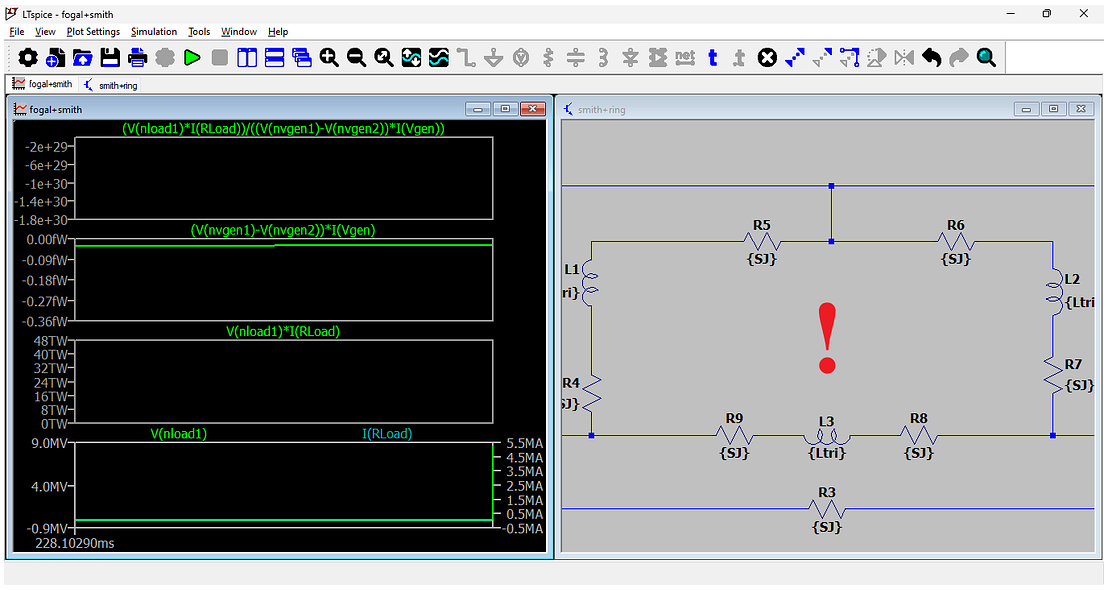
Surprise, surprise! No shorted transistor!

A delta configuration of a ring of three coils and a ring of three parallel wires (same as in previous versions of this circuit), but no central transistor to short out.

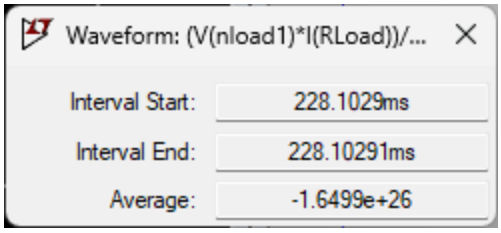
Here's the last moment of a ten-nanosecond window between 228.1029 milliseconds and 228.10291 milliseconds:



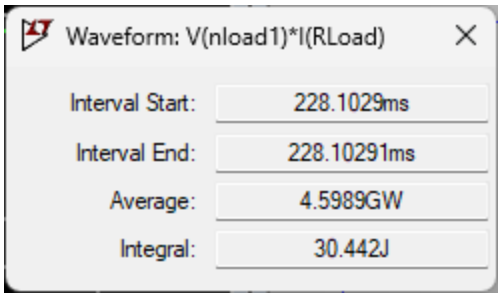
LOOK, MA, NO TRANSISTOR TO SHORT OUT!

Here's the output data for this narrow snapshot of time:

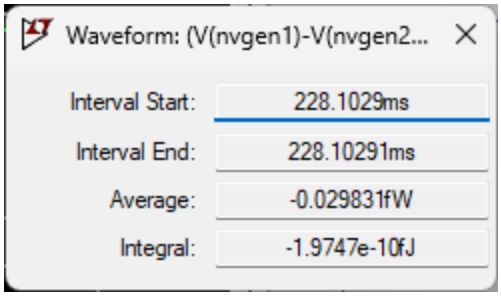
A COP (coefficience of performance) of output versus input of negative 1.65 times 10 to the power of 26 to one!



This COP is computed from an output wattage of 4.6 Giga watts!

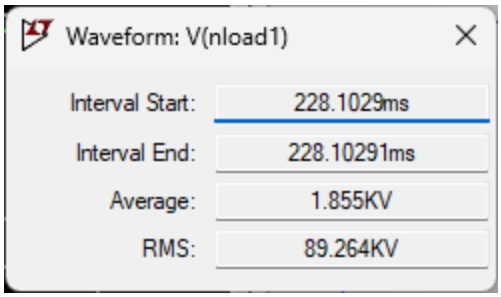


This output wattage is divided by an input wattage of negative three times ten to the power of negative 17 (which is another way of saying negative 30 atto watts!

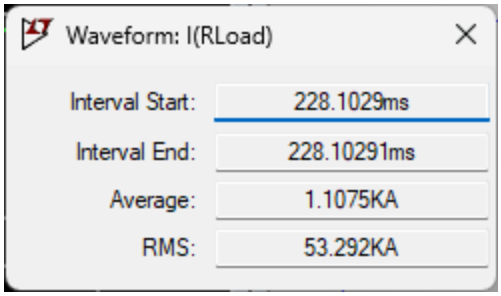


> An attowatt (aW) is a unit of power equal to 10^{-18} watts, representing one quintillionth of a watt.

The average voltage reached a peak of nearly 2 kilovolts:

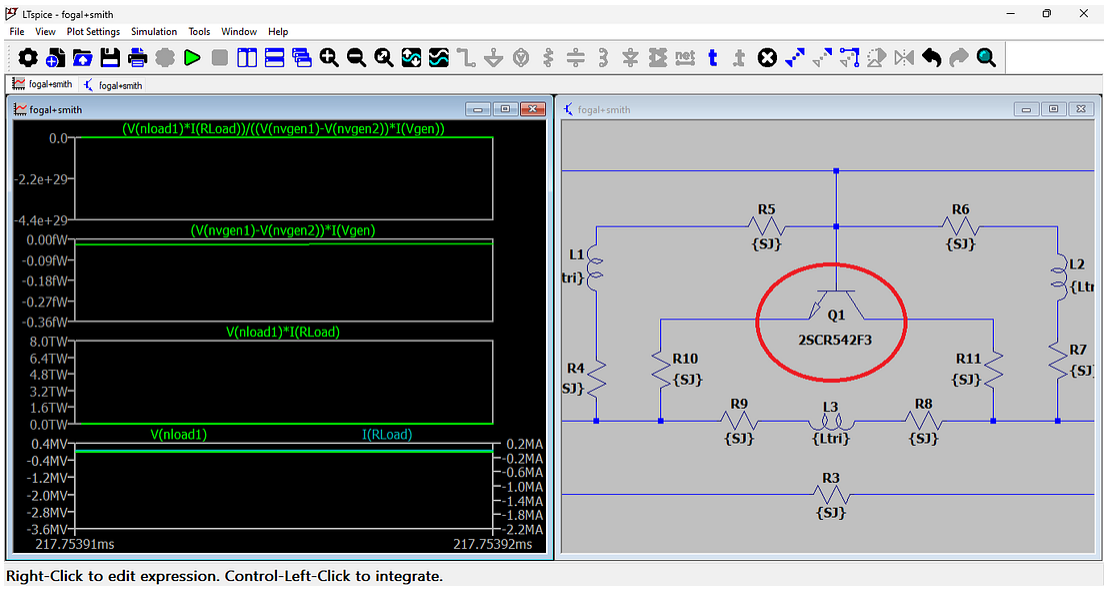


And an average current of slightly over 1 kiloamps:

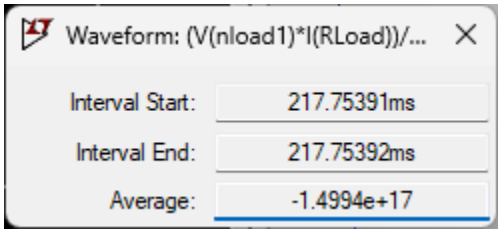


Notice how the average volts and the average amps don't equal their RMS values? This is due to the missing central transistor which had kept the sine wave characteristic output intact. This had preserved maximum power transfer. Without it, efficiency drops off. But at least this demonstrates that overunity no longer requires this transistor.

Let's see what happens when it's put back into its previous position ...



Here's the new COP:

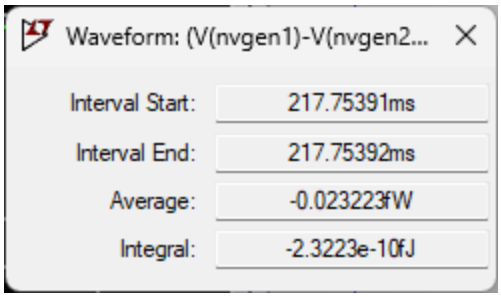


Notice how it's reduced from the previous COP, up-above, which was a billion times greater at negative 1.65 times 10 to the power of 26 to one. But this is shy by nine zeros (1e26 minus 1e17 equals 1e9).

In both instances, the simulation exploded before I could reach a favorable output range. But in this instance, it suddenly explodes with greater force making it even more difficult to be practical at regulating the outcome.

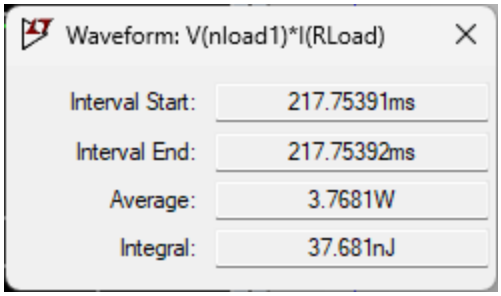
Here's the remainder of the data …

The input power during the last moment is:



23 atto watts isn't much different than the 30 atto watts, up-above, and in the same time frame of around 220 milliseconds.

Here's the output:

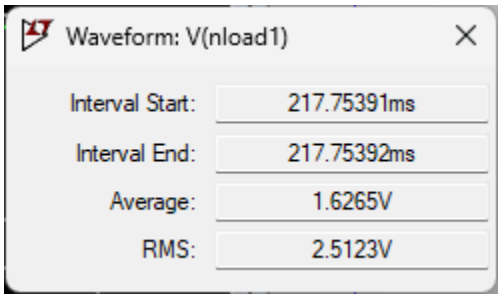


Notice it's a mere 4 watts. That's far less than the 4.6 Giga watts, up-above. That's due to this being mostly real power which is dissipating probably as the result of being an artifact of a mere surge, or periodic surging spikes. Those Giga watts, up-above, were the result of a predominance of imaginary power which cannot dissipate (unlike real power which readily dissipates). In fact, without dissipation, we'd never be able to spend power to get any benefit from it.

So, the dissipation of entropic real power is the conventional method of our enjoyment of energy while the non-dissipation of negentropic imaginary power is its accumulation.

Here's the evidence for the status of real power when simulated under the presence of this central transistor ...

The voltage at the load is:

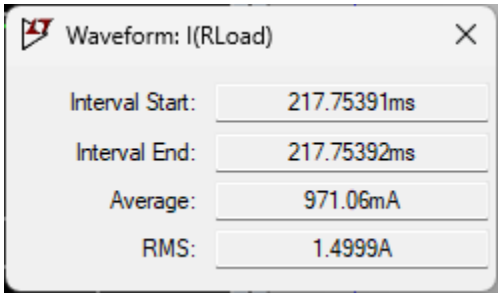


Nearly the same per its average versus its RMS average. This is due to the sine wave form of its dissipation. In earlier versions of my foray into attempting to replicate (with off the shelf parts) the customized electrolytic capacitor of William Jay Fogal, I was able to produce sine waves which did not dissipate.

But in this instance, the load is located within Donald Smith's AC to DC converter in which sine waves are not supposed to exist (at least not in their normal format). So, it's not surprising that the average voltage and the RMS average do not exactly match.

But they're closely similar.

Here's the amperage:



I get the suspicion that the use of Don Smith's converter is acting as a true load which is truly putting this circuit "through its paces".

Here's the netlist:

```
* C:\Users\vinya\Documents\TEMP\!_substack\fogal+smith\fogal+smith.asc
```

```
* Generated by LTspice 24.1.9 for Windows.

Vgen nVgen1 nVgen2 SINE(0 {input} {freq}) Rser={res}

Rbah nPar2 nVgen1 {bah}

RVgen2 0 nVgen2 {SJ}

R2 nPar2 N004 {SJ}

Q1 N014 N004 N013 0 2SCR542F3

R4 0 N016 {SJ}

L2 N015 N010 {Ltri} Rser={Ltri}

L1 N016 N009 {Ltri} Rser={Ltri}

L3 N018 N019 {Ltri} Rser={Ltri}

R7 nPar2 N015 {SJ}

R8 nPar2 N019 {SJ}

R9 N018 0 {SJ}

R5 N009 N004 {SJ}

R6 N004 N010 {SJ}

R10 0 N013 {SJ}

R11 nPar2 N014 {SJ}

R1 0 N004 {SJ}

R3 0 nPar2 {SJ}
```

D1 N011 N001 VS-E5PH6012

R12 0 N011 {SJ}

R13 nPar2 N012 {SJ}

R14 N020 0 {SJ}

R15 N021 nPar2 {SJ}

R16 N002 N001 1

R17 N023 N022 {SJ}

R18 N003 N002 1

R19 0 N003 {SJ}

R20 N017 N023 1

R21 0 N017 1

C1 N003 N017 10n Rser=1m

Q2 N008 N006 N003 0 2SCR542F3

Q3 N005 N007 N003 0 2SCR542F3

R22 N006 N005 {SJ}

R23 N008 N007 {SJ}

L4 N005 N017 {Ltri} Rser={Ltri}

L5 N017 N008 {Ltri} Rser={Ltri}

L6 nLoad1 0 {Ltri} Rser={Ltri}

RLoad nLoad1 0 {reg}

D2 N012 N002 VS-E5PH6012

D3 N023 N021 VS-E5PH6012

D4 N022 N020 VS-E5PH6012

.model D D

.lib C:\Users\vinya\AppData\Local\LTspice\lib\cmp\standard.dio

.model NPN NPN

.model PNP PNP

.lib C:\Users\vinya\AppData\Local\LTspice\lib\cmp\standard.bjt

.param input = 1m

.param Ltri = 10m

.param freq = 5e5

.param res = 10m

.param reg = 1.675 ; 6.9

.param bah = 3e9

.param sj = 100u

.param tA = 3.0999999

.param tB = 10

* cusp > sqrt(1/2)

```
.param cusp = 0.707106782

.param meager = 2e-9

K45 L4 L5 {meager}

K46 L4 L6 {cusp}

K56 L5 L6 {cusp}

.options reltol = 1e-4

.options plotwinsize = 0

.tran {tB}

.save V(nVgen1) V(nVgen2) I(Vgen) V(nLoad1) I(RLoad)

.backanno

.end
```

And here's a link for downloading the simulation files and screenshots for this blog.