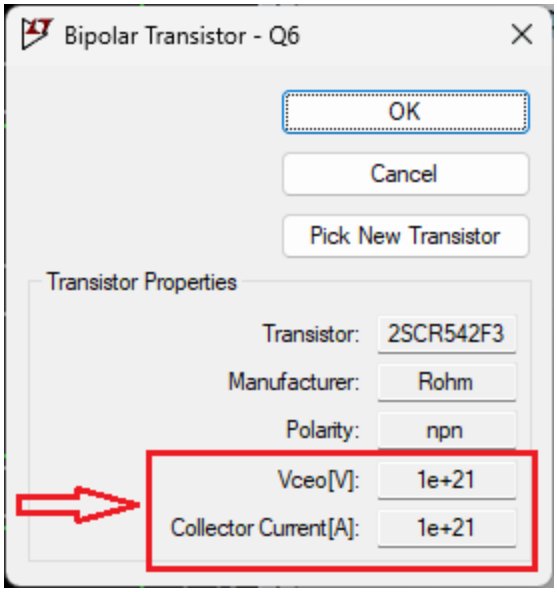
Fogal's use of a transistor may not be conventional. But choose a middle-powered transistor, and it's possible you may guarantee yourself explosive results.

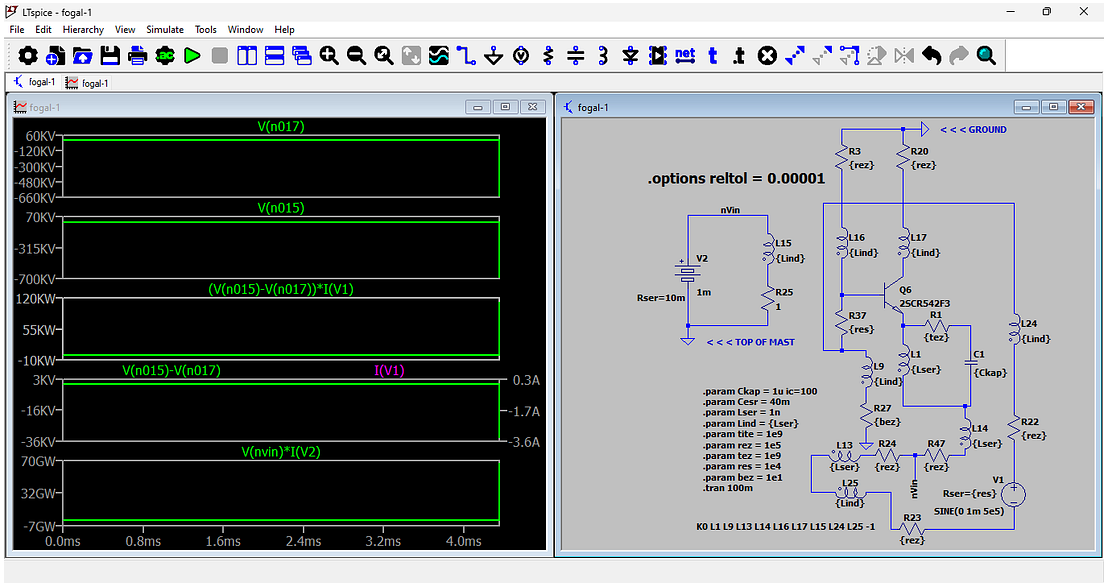
WARNING

VINYASI
MAY 08, 2026

I've modified my stance on the Charge-Barrier Transistor of William Jay Fogal due to removing the neon bulb and swapping out a standard transistor only to replace it with another variety which can withstand very large currents according to its listing inside of the LTSpice software. But, according to the company's website, it's a middle power transistor made by Rohm:

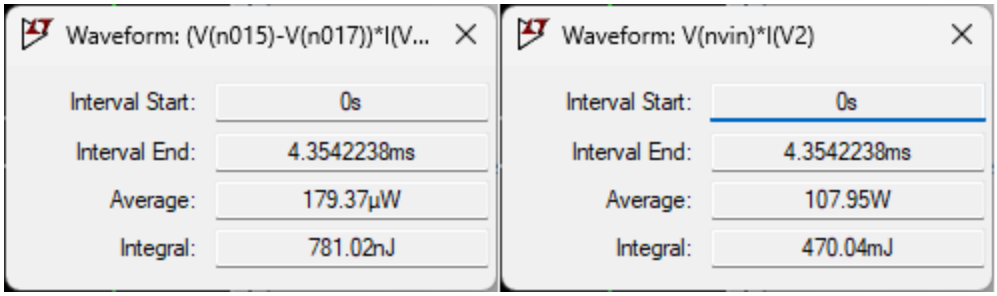


This guarantees an explosive behavior, especially if reltol is reduced below its default setting of: 0.001 to something like: 0.00001. That's 100 orders of magnitude smaller.



Notice how simple this circuit is? It has only one transistor module!

And it's fast, too. It achieves a fatal error during runtime in only 4.35 milliseconds as is recorded in the outputs for its two voltage sources: its V1 sine wave frequency generator on the left and its V2 battery/mast on the right (in the next screenshot):



Notice how both wattages (which are averages) are of a positive mathematical polarity of sign indicating that they are *not generating*

power. Instead, they're *absorbing power* indicating that power is coming from **somewhere else in the circuit** outside of its sources.

That's cool!

I think this circuit is all about its transistor. In other words, fabricate a unique set of parameters for this transistor, and this circuit configuration will deliver whatever you want: pulsations or an explosion. In this case, it's a guaranteed explosion.

At least, that's my guess given the evidence and my limited expertise.

Here's the download link for this circuit's files.

And here's its netlist:

```
* D:\Documents\Sims\LTSpice\2026\05 - May\07\fogal-1.asc

* Generated by LTspice 24.1.9 for Windows.

L1 N007 N010 {Lser} Rser={Lser}

R1 N008 N007 {tez}

R3 0 N002 {rez}

V1 N015 N017 SINE(0 1m 5e5) Rser={res}

R37 N001 N006 {res}

R47 N014 nVin {rez}

R20 0 N003 {rez}

R22 N011 N015 {rez}

R23 N017 N016 {rez}
```

R24 nVin N013 {rez}

V2 nVin 0 1m Rser=10m

R25 N005 0 1

R27 0 N009 {bez}

L9 N001 N009 {Lind} Rser={Lind}

L13 N013 N012 {Lser} Rser={Lser}

L14 N010 N014 {Lser} Rser={Lser}

L15 nVin N005 {Lind} Rser={Lind}

L16 N002 N006 {Lind} Rser={Lind}

L17 N003 N004 {Lind} Rser={Lind}

L24 N001 N011 {Lind} Rser={Lind}

L25 N016 N012 {Lind} Rser={Lind}

C1 N008 N010 {Ckap} Rser={Cesr}

Q6 N004 N006 N007 0 2SCR542F3

.model NPN NPN

.model PNP PNP

.lib C:\Users\vinya\AppData\Local\LTspice\lib\cmp\standard.bjt

.param Ckap = 1u ic=100

.param Cesr = 40m

.param Lser = 1n

.param Lind = {Lser}

.param tite = 1e9

.param rez = 1e5

.param tez = 1e9

.param res = 1e4

.param bez = 1e1

.tran 100m

K0 L1 L9 L13 L14 L16 L17 L15 L24 L25 -1

.options reltol = 0.00001

* < < < GROUND

* < < < TOP OF MAST

.backanno

.end

Here’s the log file contents:

LTspice 24.1.9 for Windows

Circuit: D:\Documents\Sims\LTSpice\2026\05 - May\07\fogal-1.net

Start Time: Thu May 7 19:15:45 2026

Options: reltol = 0.00001

solver = Normal

Maximum thread count: 4

tnom = 27

temp = 27

method = trap

reltol = 1e-05

Early termination of direct N-R iteration.

Direct Newton iteration failed to find .op point. (Use ".option noopiter" to skip.)

Starting Gmin stepping

Gmin = 10

Gmin = 1.07374

Gmin = 0.115292

Gmin = 0.0123794

Gmin = 0.00132923

Gmin = 0.000142725

Gmin = 1.5325e-05

Gmin = 1.6455e-06

Gmin = 1.76685e-07

Gmin = 1.89714e-08

Gmin = 2.03704e-09

Gmin = 2.18725e-10

Gmin = 2.34854e-11

Gmin = 2.52173e-12

Gmin = 2.70769e-13

Gmin = 0

Gmin stepping succeeded in finding the operating point.

Warning: Simulation tolerance relaxed to achieve convergence from 4.3542237751188250e-03

Convergence Failure: Time step too small; time = 0.00435422, timestep = 1.25019e-18: trouble with node “n007”

Simulation Failed: Iteration limit reached

Total elapsed time: 7.235 seconds.

Files loaded:

D:\Documents\Sims\LTSpice\2026\05 - May\07\fogal-1.net

C:\Users\vinya\AppData\Local\LTspice\lib\cmp\standard.bjt

Here is some more information I found on the inventor and his device:

INVENTORS FROM A to H (translated from French into English):

233 Bobby Jones Expressway, Martinez, CA 30907

Inventor of a device bearing his name, an amplifier without moving parts, he is a colleague whom Bearden says is very close to him.

U.S. Patents Nos. 5,196,809 and 5,430,413

Us5196809
987KB PDF file

Download

Us5430413
1.08MB PDF file

Download

He patented the world's first dq/dt-blocking semiconductor ("degenerate" semiconductor or Fogal chip) that partially blocks normal current while continuing to pass the flow of voltage. Bearden has published a technical explanation of this semiconductor that uses an extremely little-known characteristic called *"overpotential"* and known to a few chemists who specialize in electrode effects, including Bernhardt Patrick John O'Mara Bockris, the world's leading expert on this theory.

The '94 patent application, describes methods and practices of the fundamental process of load blocking in order to obtain super-unit electric power systems.

He obtained two patents in 1993 and 1995 on a faster, high-gain, low-distortion switch transistor, and in January 1996, together with Bearden, he filed an application patent for processes and devices that insert signals, including all desired bandwidths, within a DC voltage in a scalar potential through a specific use of the Fogal semiconductor.

See the article The Truth Behind Charged Barrier Technology with comments by Colonel Tom Bearden in:
http://www.eskimo.com/~ghawk/fogal_device/notes.htm
http://www.eskimo.com/~ghawk/fogal_device/

and also, The Trailer for "Petrovoltaics", Part 12 in the "Energy from the Vacuum" Science Series of DVDs.