Success! Finally, Explosive Fogal without Fatal Simulator Error!

That's a big deal.

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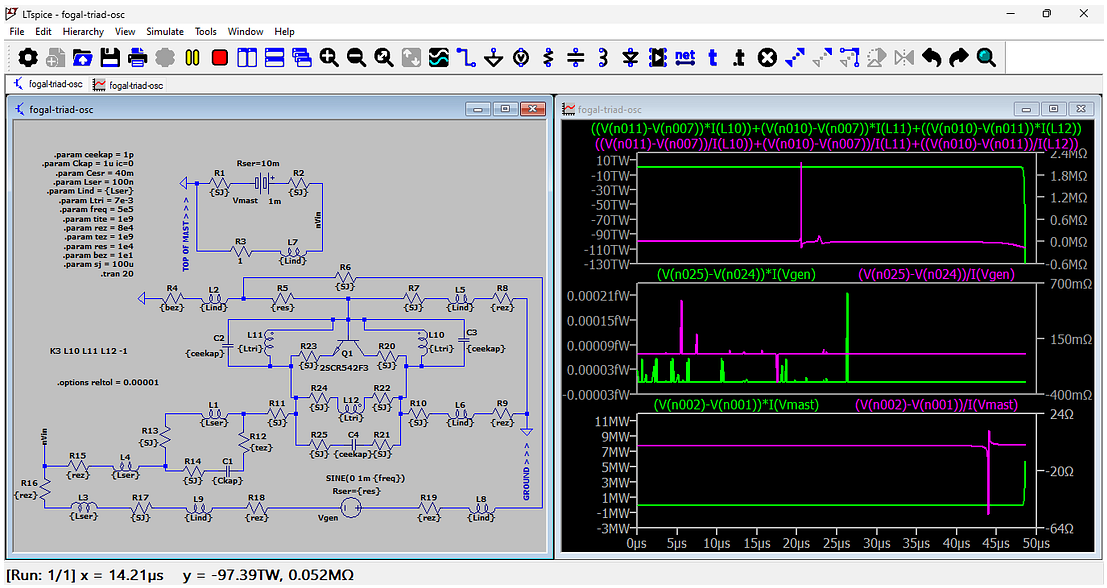
MAY 10, 2026

I have not succeeded yet to prevent William Jay Fogal’s Charge Barrier Transistor from blowing up. But I’ve succeeded in reducing simulator errors which mainly are due to the abrupt escalation of amplitude, at an exponential rate, which the simulator can’t tolerate. But by smoothing this out, fatal errors have disappeared and non-fatal errors are reduced. Whew! One significant baby step forward.

Coils continue to put out negative watts measuring: -129.15TW at the moment the simulator slowed down its calculations to a crawl. The “Vmast” source continues to absorb positive watts at: +5.8198MW. The “Vgen” source stops absorbing and fails to generate (somewhere around 50 microseconds into runtime) measuring zero watts, but that’s OK so long as the mast continues to absorb power.



And all of this because of shorting out the three terminals of the transistor, Q1, with three coil/cap pairs and magnetically coupling these three coils together and decoupling all of the other coils from each other and from every other coil, thus, magnetically isolating them, all, from each other.

Download this circuit simulation.

Netlist:

* D:\Documents\Sims\LTSpice\2026\05 - May\10\fogal-triad-osc.asc

* Generated by LTspice 24.1.9 for Windows.

L1 N017 N016 {Lser} Rser={Lser}

R12 N025 N017 {tez}

R8 0 N009 {rez}

Vgen N031 N030 SINE(0 1m {freq}) Rser={res}

R5 N004 N007 {res}

R15 nVin N022 {rez}

R9 0 N019 {rez}

R19 N032 N031 {rez}

R18 N029 N030 {rez}

R16 N026 nVin {rez}

Vmast N002 N001 1m Rser=10m

R3 N003 0 1

R4 0 N006 {bez}

L2 N004 N006 {Lind} Rser={Lind}

L3 N026 N027 {Lser} Rser={Lser}

L4 N023 N022 {Lser} Rser={Lser}

L7 nVin N003 {Lind} Rser={Lind}

L5 N009 N008 {Lind} Rser={Lind}

L6 N019 N018 {Lind} Rser={Lind}

L8 N005 N032 {Lind} Rser={Lind}

L9 N029 N028 {Lind} Rser={Lind}

C1 N025 N024 {Ckap} Rser={Cesr}

Q1 N012 N007 N011 0 2SCR542F3

R2 nVin N002 {SJ}

R1 N001 0 {SJ}

R17 N028 N027 {SJ}

R14 N024 N023 {SJ}

R7 N008 N007 {SJ}

R10 N018 N013 {SJ}

R13 N023 N016 {SJ}

R6 N005 N004 {SJ}

R11 N010 N017 {SJ}

L10 N013 N007 {Ltri} Rser={Ltri}

L11 N010 N007 {Ltri} Rser={Ltri}

L12 N014 N015 {Ltri} Rser={Ltri}

C2 N007 N010 {ceekap} Rser={Cesr}

C3 N007 N013 {ceekap} Rser={Cesr}

C4 N021 N020 {ceekap} Rser={Cesr}

R20 N013 N012 {SJ}

R21 N013 N021 {SJ}

R22 N013 N015 {SJ}

R23 N011 N010 {SJ}

R24 N014 N010 {SJ}

R25 N020 N010 {SJ}

.model NPN NPN

.model PNP PNP

.lib C:\Users\vinya\AppData\Local\LTspice\lib\cmp\standard.bjt

.param ceekap = 1p

.param Ckap = 1u ic=0

.param Cesr = 40m

.param Lser = 100n

.param Lind = {Lser}

.param Ltri = 7e-3

.param freq = 5e5

.param tite = 1e9

.param rez = 8e4

.param tez = 1e9

.param res = 1e4

.param bez = 1e1

.param sj = 100u

.tran 20

.options reltol = 0.00001

* GROUND > > >

* TOP OF MAST > > >

K3 L10 L11 L12 -1

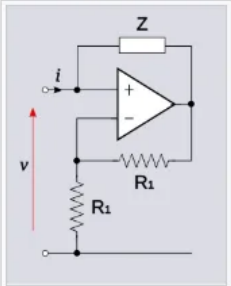
.backanno

.end

Reference:

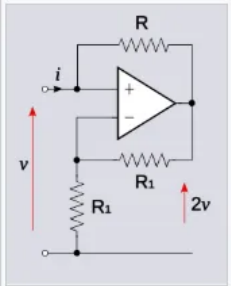
The Negative Impedance Converter of William Jay Fogal’s Nonlinear, Charged-Barrier Transistor but without the Linear Pumping of an OpAmp.

VINYASI · MAY 9



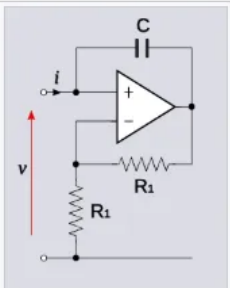
Negative impedance circuit

$$Z_{\text{in}} = \frac{v}{i} = -Z$$



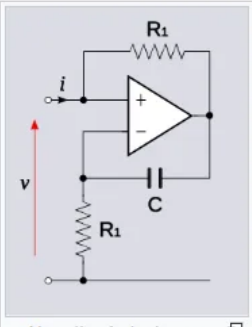
Negative resistance circuit

$$R_{\text{in}} = \frac{v}{i} = -R$$



Negative capacitance circuit

$$Z_{\text{in}} = \frac{v}{i} = \frac{j}{\omega C}$$



Negative inductance circuit

$$Z_{\text{in}} = \frac{v}{i} = -j\omega C R_1^2$$

We may already be familiar with the concept of a negative impedance converter. Wikipedia enlightens us about its nature by giving us examples of circuits – all of which are composed of opamps which r...

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