

Success! I've Figured out How to Turn OFF Fogal's Charge Barrier Transistor to Halt its Persistent Explosive Tendency ...

... by removing merely one coil from the magnetic coupling among its central triad of coils which short out (surround) its transistor.



VINYASI

MAY 11, 2026

This works like a charm! And, I can add more coils — in parallel with the triad and it works the same way: if I magnetically couple all of them, except one coil, then this circuit's explosive escalation towards self-annihilation never happens. Instead, a meager output results.

To measure this condition, and keep track of it, I've elected to focus merely on the two voltage sources which supply this circuit with energy. For, if either one of them significantly explodes in the positive direction of wattage, then I know that this circuit has not been turned OFF but remains ON because that positive wattage indicates the absorption of power. But if both voltage sources put out energy in the femto range (of 10 raised to the power of negative 15-ish), and this output is negative (not positive), then I know that this circuit's overunity is turned OFF since neither of its voltage sources are absorbing any power which might have been excessively generated by this circuit if it had been in overunity mode. Instead, this negative condition of wattage at both voltage sources indicates that both of them are generating power and not much at that!

Hallelujah! Whoopee Doodah!

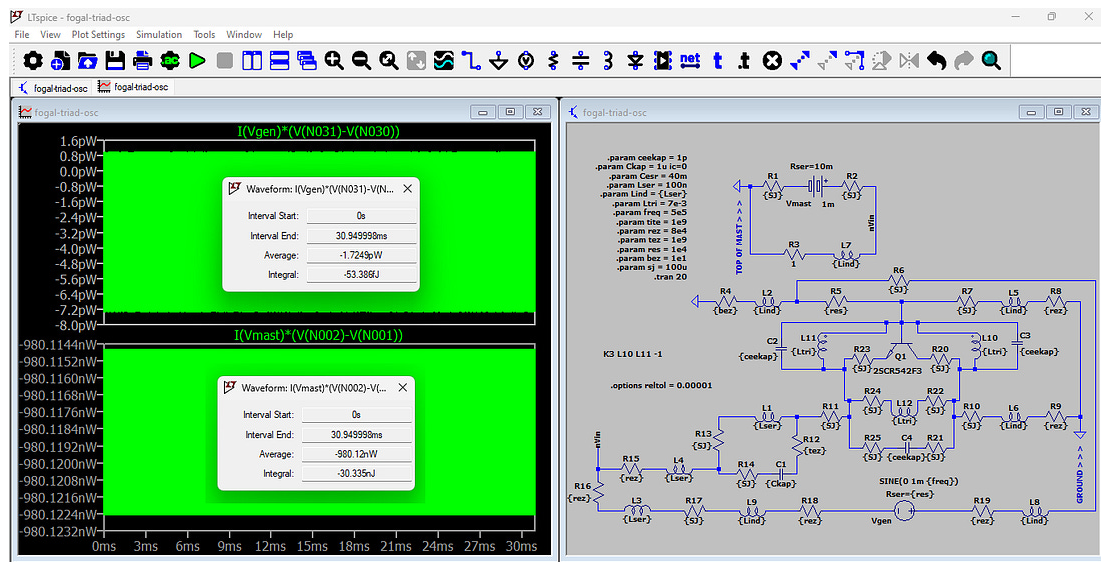
We can further stipulate that the voltage source which is labeled: 'Vmast' is a grounded aerial. It's positive polarity of sign (during its ON condition) indicates that it is broadcasting that much positive wattage into its immediate environment which could disturb local radio reception and attract the attention of the FCC if left ON for any lengthy duration.

Meanwhile, the voltage source labeled: 'Vgen' becomes a motor whenever it is absorbing positive polarity of signed wattage whenever during this circuit's ON condition. So, we may designate this to be an inductive load.

Here are some examples:

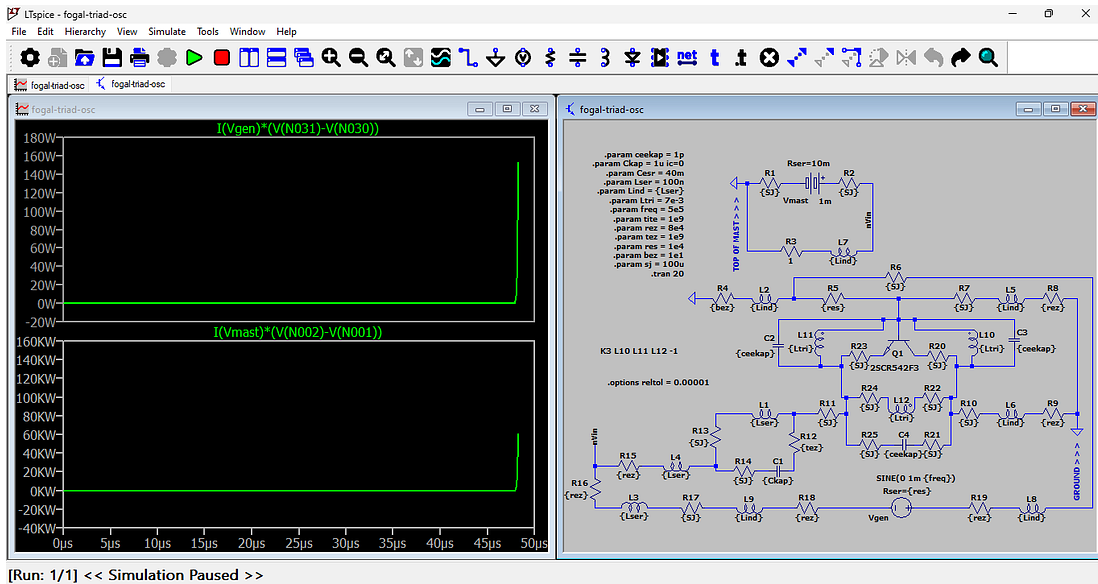
Example #1

OFF



Right-Click to edit expression. Control-Left-Click to integrate. Alt-Left-Click to reverse cross probe Vgen.

ON



'OFF' Netlist:

* D:\Documents\Sims\LTSpice\2026\05 - May\11\fogal-triad-osc-OFF.asc

* Generated by LTSpice 24.1.9 for Windows.

L1 N017 N016 {Lser} Rser={Lser}

R12 N025 N017 {tez}

R8 0 N009 {rez}

Vgen N031 N030 SINE(0 1m {freq}) Rser={res}

R5 N004 N007 {res}

R15 nVin N022 {rez}

R9 0 N019 {rez}

R19 N032 N031 {rez}

R18 N029 N030 {rez}

R16 N026 nVin {rez}
Vmast N002 N001 1m Rser=10m
R3 N003 0 1
R4 0 N006 {bez}
L2 N004 N006 {Lind} Rser={Lind}
L3 N026 N027 {Lser} Rser={Lser}
L4 N023 N022 {Lser} Rser={Lser}
L7 nVin N003 {Lind} Rser={Lind}
L5 N009 N008 {Lind} Rser={Lind}
L6 N019 N018 {Lind} Rser={Lind}
L8 N005 N032 {Lind} Rser={Lind}
L9 N029 N028 {Lind} Rser={Lind}
C1 N025 N024 {Ckap} Rser={Cesr}
Q1 N012 N007 N011 0 2SCR542F3
R2 nVin N002 {SJ}
R1 N001 0 {SJ}
R17 N028 N027 {SJ}
R14 N024 N023 {SJ}
R7 N008 N007 {SJ}

R10 N018 N013 {SJ}

R13 N023 N016 {SJ}

R6 N005 N004 {SJ}

R11 N010 N017 {SJ}

L10 N013 N007 {Ltri} Rser={Ltri}

L11 N010 N007 {Ltri} Rser={Ltri}

L12 N014 N015 {Ltri} Rser={Ltri}

C2 N007 N010 {ceekap} Rser={Cesr}

C3 N007 N013 {ceekap} Rser={Cesr}

C4 N021 N020 {ceekap} Rser={Cesr}

R20 N013 N012 {SJ}

R21 N013 N021 {SJ}

R22 N013 N015 {SJ}

R23 N010 N011 {SJ}

R24 N014 N010 {SJ}

R25 N020 N010 {SJ}

.model NPN NPN

.model PNP PNP

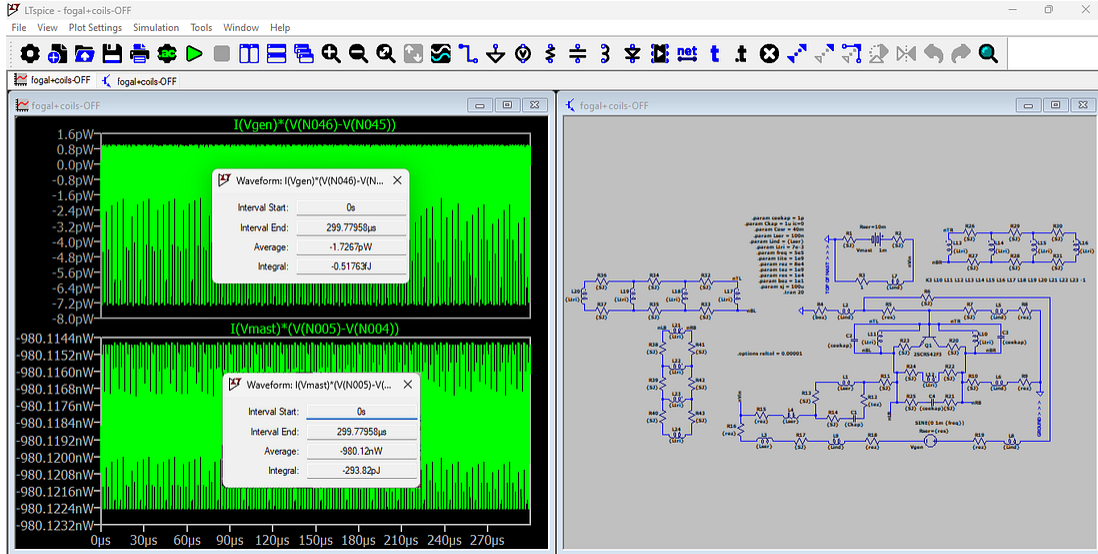
.lib C:\Users\vinya\AppData\Local\LTspice\lib\cmp\standard.bjt

```
.param ceekap = 1p
.param Ckap = 1u ic=0
.param Cesr = 40m
.param Lser = 100n
.param Lind = {Lser}
.param Ltri = 7e-3
.param freq = 5e5
.param tite = 1e9
.param rez = 8e4
.param tez = 1e9
.param res = 1e4
.param bez = 1e1
.param sj = 100u
.tran 20
.options reltol = 0.00001
* GROUND > > >
* TOP OF MAST > > >
K3 L10 L11 -1
.backanno
```

.end

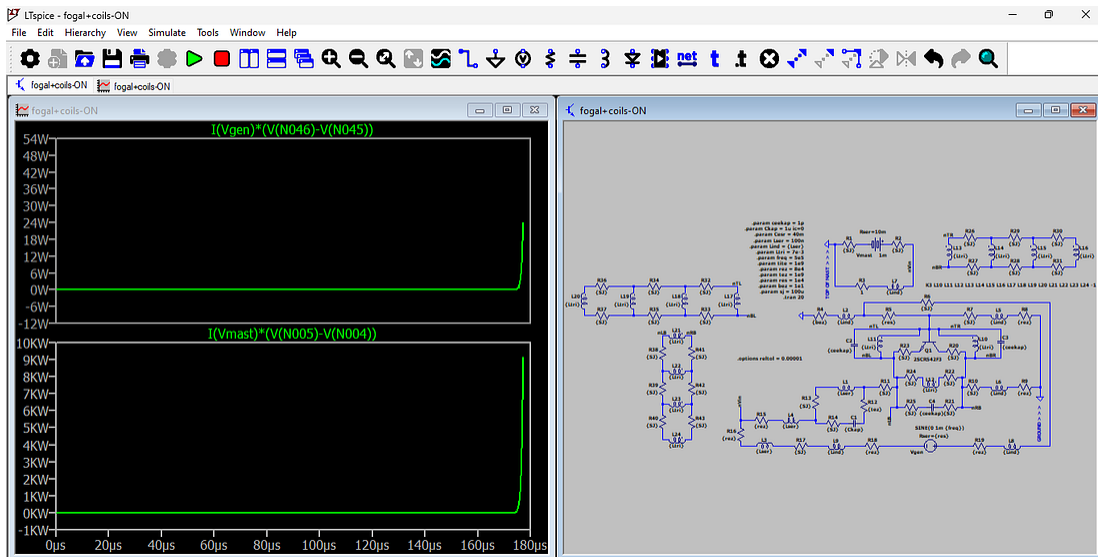
Example #2

OFF



Right-Click to edit expression. Control-Left-Click to integrate. Alt-Left-Click to reverse cross probe Vgen.

ON



[Run: 1/1] << Simulation Paused >>

'OFF' Netlist:

* D:\Documents\Sims\LTSpice\2026\05 - May\11\fogal+coils-OFF.asc

* Generated by LTSpice 24.1.9 for Windows.

L1 N028 N027 {Lser} Rser={Lser}

R12 N038 N028 {tez}

R8 0 N020 {rez}

Vgen N046 N045 SINE(0 1m {freq}) Rser={res}

R5 N013 nTR {res}

R15 nVin N035 {rez}

R9 0 N030 {rez}

R19 N047 N046 {rez}

R18 N044 N045 {rez}

R16 N041 nVin {rez}

Vmast N005 N004 1m Rser=10m

R3 N012 0 1

R4 0 N018 {bez}

L2 N013 N018 {Lind} Rser={Lind}

L3 N041 N042 {Lser} Rser={Lser}

L4 N036 N035 {Lser} Rser={Lser}

L7 nVin N012 {Lind} Rser={Lind}

L5 N020 N019 {Lind} Rser={Lind}

L6 N030 N029 {Lind} Rser={Lind}

L8 N014 N047 {Lind} Rser={Lind}

L9 N044 N043 {Lind} Rser={Lind}

C1 N038 N037 {Ckap} Rser={Cesr}

Q1 N022 nTR N021 0 2SCR542F3

R2 nVin N005 {SJ}

R1 N004 0 {SJ}

R17 N043 N042 {SJ}

R14 N037 N036 {SJ}

R7 N019 nTR {SJ}

R10 N029 nRB {SJ}

R13 N036 N027 {SJ}

R6 N014 N013 {SJ}

R11 nLB N028 {SJ}

L10 nRB nTR {Ltri} Rser={Ltri}

L11 nLB nTR {Ltri} Rser={Ltri}

L12 N025 N026 {Ltri} Rser={Ltri}

C2 nTR nLB {ceekap} Rser={Cesr}

C3 nTR nRB {ceekap} Rser={Cesr}

C4 N034 N033 {ceekap} Rser={Cesr}

R20 nRB N022 {SJ}

R21 nRB N034 {SJ}

R22 nRB N026 {SJ}

R23 nLB N021 {SJ}

R24 N025 nLB {SJ}

R25 N033 nLB {SJ}

L13 nRB nTR {Ltri} Rser={Ltri}

L14 N006 N001 {Ltri} Rser={Ltri}

L15 N007 N002 {Ltri} Rser={Ltri}

L16 N008 N003 {Ltri} Rser={Ltri}

L17 nLB nTR {Ltri} Rser={Ltri}

L18 N017 N011 {Ltri} Rser={Ltri}

L19 N016 N010 {Ltri} Rser={Ltri}

L20 N015 N009 {Ltri} Rser={Ltri}

L21 nLB nRB {Ltri} Rser={Ltri}

L22 N023 N024 {Ltri} Rser={Ltri}

L23 N031 N032 {Ltri} Rser={Ltri}

L24 N039 N040 {Ltri} Rser={Ltri}

R26 N001 nTR {SJ}

R27 N006 nRB {SJ}

R28 N007 N006 {SJ}

R29 N002 N001 {SJ}

R30 N003 N002 {SJ}

R31 N008 N007 {SJ}

R32 nTR N011 {SJ}

R33 nLB N017 {SJ}

R34 N011 N010 {SJ}

R35 N017 N016 {SJ}

R36 N010 N009 {SJ}

R37 N016 N015 {SJ}

R38 N023 nLB {SJ}

R39 N031 N023 {SJ}

R40 N039 N031 {SJ}

R41 N024 nRB {SJ}

R42 N032 N024 {SJ}

R43 N040 N032 {SJ}

.model NPN NPN

.model PNP PNP

.lib C:\Users\vinya\AppData\Local\LTspice\lib\cmp\standard.bjt

.param ceekap = 1p

.param Ckap = 1u ic=0

.param Cesr = 40m

.param Lser = 100n

.param Lind = {Lser}

.param Ltri = 7e-3

.param freq = 5e5

.param tite = 1e9

.param rez = 8e4

.param tez = 1e9

.param res = 1e4

.param bez = 1e1

.param sj = 100u

.tran 20

.options reltol = 0.00001

* GROUND > > >

* TOP OF MAST > > >

K3 L10 L11 L12 L13 L14 L15 L16 L17 L18 L19 L20 L21 L22 L23 -1

.backanno

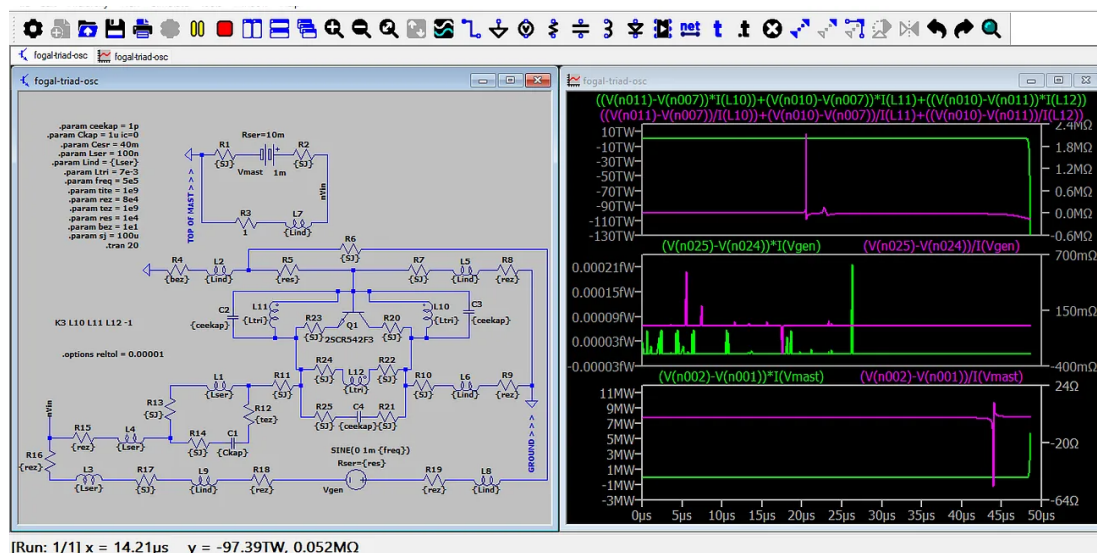
.end

[Download these circuits.](#)

Previous post in this series:

Success! Finally, Explosive Fogal without Fatal Simulator Error!

VINYASI · MAY 10



I have not succeeded yet to prevent William Jay Fogal's Charge Barrier Transistor from blowing up. But I've succeeded in reducing simulator errors which mainly are due to the abrupt escalation of amp...

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